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EXAMINER	
MCLEAN, NEIL R	

ART UNIT	PAPER NUMBER
2625	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/615,738	TWEDE, ROGER S.	
	Examiner	Art Unit	
	Neil R. McLean	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *29-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☒ Claim(s) *1-3,16-19 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/09/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 29-33 are drawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claims. Applicant timely traversed the restriction (election) requirement in the reply filed on 10/08/2007.

Applicant's election with traverse of Election/Restriction in the reply filed on 10/08/2007 is acknowledged. The traversal is on the ground(s) that the inventions are not patentably distinct. This is not found persuasive because Invention I is drawn to Graphics Processing and Visual Display Attributes, and Invention II is drawn to a Printing Device and Memory. If Invention I where cancelled, Invention II could still be patentable if found to be patentable. Also, they are claims in independent form, claiming two distinct inventions. Please refer to MPEP 806.05 (c)

The requirement is still deemed proper and is therefore made FINAL.

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested:

FRAME BUFFER FOR A SERIALLY ADDRESSABLE DISPLAY

2. The abstract of the disclosure is objected to because of the phrase 'non-direct memory access (DMA) display' and 'non DMA display'. Applicant is reminded of the proper language, content and format for an abstract of the disclosure.

The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains, not what the invention does not contain.

Correction is required. See MPEP § 608.01(b).

Drawings

3. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because of the term 'non-DMA display'. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The

corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Objections

4. Claims 1-3, 16-19, and 22 are objected to because of the following informalities: The phrase 'non-direct memory access (DMA) display' and 'non-DMA display' is not descriptive of the invention. Please say what the invention does, not what it does not do. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1-3, and 5-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshiba (US 4,816,815).

Regarding Claim 1:

Yoshiba discloses a system comprising:

a frame buffer memory (e.g., VRAM #1 in Figure 1) for a serially addressable (Column 4, lines 59-65), non-direct memory access (DMA) display (e.g., CRT 10 in Figure 1), the frame buffer memory having a number of pixels corresponding to a number of pixels of the non-DMA display (Column 6, lines 38-41); and,

a display data transfer circuit (e.g. Controller 22 shown in Figure 1) to serially transfer (See Parallel to Serial Converter 176 to Video transfer in Figure 5) the pixels of the frame buffer memory to the non-DMA display to update (The process of Figure 5; Described in Column 6, lines 16-26) the non-DMA display.

Regarding Claim 2:

Yoshiba discloses the system of claim 1, further comprising the non-DMA display (e.g., CRT 10 in Figure 1).

Regarding Claim 3:

The system of claim 1, wherein the non-DMA display is communicated with via a communication format comprising:

an x coordinate of the display (The portion of the address read out from e.g., VRAM 16 which corresponds to the x position of the display);

a y coordinate of the display (The portion of the address read out from e.g., VRAM 16 which corresponds to the y coordinate of the display); and,

a number of sequential pixels to be written to the display starting at the x coordinate and at the y coordinate (The process described in Column 6, lines 34-

41 wherein the display data is transferred).

Regarding Claim 5:

The system of claim 1, wherein the frame buffer memory (e.g., VRAM #1 in Figure 1 is separate from controller 22 in Figure 1) is separate from the display data transfer circuit.

Regarding Claim 6:

The system of claim 1, wherein the frame buffer memory (e.g., VRAM #2 in Figure 1) is part of the display data transfer circuit (e.g. Display Switching Circuit 156 shown in Figure 6; Column 5, lines 5-10).

Regarding Claim 7:

The system of claim 1, wherein the data transfer circuit is an application-specific integration circuit (ASIC) (e.g. Display Switching Circuit 156 shown in Figure 6; Column 5, lines 5-10).

Regarding Claim 8:

The system of claim 1, wherein the frame buffer memory has a bit depth of at least one bit corresponding to a bit depth of the display (Column 9, lines 44-51).

Regarding Claim 9:

The system of claim 1, wherein the display data transfer circuit is to start at an origin point of the display when serially transferring the pixels of the frame buffer memory to the display (Column 9, lines 44-51).

Regarding Claim 10:

The system of claim 1, wherein the display data transfer circuit is to monitor changes made to the pixels of the frame buffer memory, and is to serially transfer the pixels of the frame buffer memory that have changed to the display (Column 9, lines 44-51).

Regarding Claim 11:

The system of claim 10, wherein the display data transfer circuit is to serially transfer the pixels of the frame buffer memory that have changed to the display by determining a number of sequential pixel groups inclusive of one or more of the pixels of the frame buffer memory that have changed that minimize data transfer to the display (Column 9, lines 44-51).

Regarding Claim 12:

The system of claim 11, wherein at least one of the sequential pixel groups are also inclusive of one or more of the pixels of the frame buffer memory that remain unchanged (Column 9, lines 44-51).

Regarding Claim 13:

The system of claim 10, wherein the frame buffer memory is a first frame buffer memory (e.g., VRAM #1 in Figure 1), the system further comprising a second frame buffer memory (e.g,. VRAM #2 in Figure 1) to which the pixels of the first frame buffer memory are copied, the display data transfer circuit to compare pixels of the second frame buffer memory against the pixels of the first frame buffer memory to determine whether changes have been made to the pixels of the first frame buffer memory (Column 8, line 66 – Column 9, line 7).

Regarding Claim 14:

The system of claim 10, further comprising a mask (Column 7, lines 45-55) to indicate that changes have been made to the pixels of the frame buffer memory.

Regarding Claim 15:

The system of claim 1, wherein the frame buffer memory supports at least one of an endianness selector and a bit directional selection capability (Column 9, lines 44-51).

Regarding Claim 16:

Yoshiba discloses a system comprising:

a frame buffer memory (e.g., VRAM #1 in Figure 1) for a serially addressable (Column 4, lines 59-65), non-direct memory access (DMA) display (e.g., CRT 10 in Figure 1), the frame buffer memory having a number of pixels

corresponding to a number of pixels of the non-DMA display (Column 6, lines 38-41); and,

means (The device or circuit portion of the Controller 22 shown in Figure 1) for serially transferring (See Parallel to Serial Converter 176 to Video transfer in Figure 5) the pixels of the frame buffer memory to the non-DMA display to update (The process of Figure 5; Described in Column 6, lines 16-26) the non-DMA display.

Regarding Claim 17:

The system of claim 16, further comprising the non-DMA display (e.g., CRT 10 in Figure 1).

Regarding Claim 18:

The system of claim 16, wherein the non-DMA display is communicated with via a communication format comprising:

an x coordinate of the display (The portion of the address read out from e.g., VRAM 16 which corresponds to the x position of the display);

a y coordinate of the display (The portion of the address read out from e.g., VRAM 16 which corresponds to the y coordinate of the display); and,

a number of sequential pixels to be written to the display starting at the x coordinate and at the y coordinate (The process described in Column 6, lines 34-41 wherein the display data is transferred).

Regarding Claim 19:

The system of claim 16, wherein the means is further for monitoring changes made to the pixels of the frame buffer memory, and for serially transferring the pixels of the frame buffer memory that have changed to the non-DMA display as a series of pixel groups (Column 9, lines 44-51).

Regarding Claim 20:

The system of claim 19, wherein each pixel group includes one or more sequential pixels of the frame buffer memory that have changed (Column 9, lines 44-51).

Regarding Claim 21:

The system of claim 19, wherein each pixel group includes a sequence of at least one pixel, the sequence of at least one pixel group including one or more of the pixels of the frame buffer memory that remain unchanged (Column 9, lines 44-51).

Regarding Claim 22:

Yoshiba discloses a method comprising:

determining that one or more pixels of a frame buffer memory for a serially addressable, non-direct memory access (DMA) display have changed (The process of Figure 5; Described in Column 6, lines 16-26); and,

in response to determining that the one or more pixels of the frame buffer memory have changed, serially transferring (See Parallel to Serial Converter 176 to Video transfer in Figure 5) at least the one or more pixels from the frame buffer memory to the display.

Regarding Claim 23:

The method of claim 22, wherein determining that the one or more pixels of the frame buffer memory have changed comprises comparing the frame buffer memory to a previously made copy of the frame buffer memory to determine whether one or more pixels of the frame buffer memory have changed (The process described in Column 6, lines 34-41 wherein the display data is transferred).

Regarding Claim 24:

The method of claim 22, wherein determining that the one or more pixels of the frame buffer memory have changed comprises utilizing a mask indicating that the one or more pixels have changed (Column 7, lines 45-55).

Regarding Claim 25:

The method of claim 22, wherein serially transferring at least the one or more pixels from the frame buffer memory to the display comprises, for each pixel of the one or more pixels,

specifying to the display an x coordinate and a y coordinate of the pixel; and (The portion of the address read out from e.g., VRAM 16 which corresponds to the x position and the y postion of the display),

specifying the pixel to the display (The process described in Column 6, lines 34-41 wherein the display data is transferred to the display).

Regarding Claim 26:

The method of claim 22, wherein serially transferring at least the one or more pixels from the frame buffer memory to the display comprises determining a number of sequential pixel groups inclusive of at least the one or more pixels that minimize data transfer to the display (Column 9, lines 44-51).

Regarding Claim 27:

The method of claim 26, wherein determining the number of sequential pixel groups comprises determining at least one pixel group that is also inclusive of one or more pixels of the frame buffer memory that remain unchanged (Column 9, lines 44-51).

Regarding Claim 28:

The method of claim 26, wherein serially transferring at least the one or more pixels from the frame buffer memory to the display further comprises, for each sequential pixel group (Column 9, lines 44-51),

specifying to the display an x coordinate and a y coordinate at which the sequential pixel group starts (As Shown in Figure 14); and,

specifying to the display a number of bits corresponding to the sequential pixel group (As shown in Figure 14).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshiba as applied to claim 1 above, and further in view of Dunn (US 4,497,036).

Regarding Claim 4:

Yoshiba discloses the system of claim 1, wherein the non-DMA display is one of a stand alone display and an embedded display.

Yoshiba does not disclose expressly wherein the display is an embedded display.

Dunn discloses an embedded display; mounted on the inner surface of the cases cover (Column 4, lines 41-45).

Yoshiba & Dunn are combinable because they are from the same field of endeavor of image processing, e.g., a cpu coupled to and controlling a display.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have a display embedded in a computer system.

The suggestion/motivation for doing so would have been to have a means to communicate with a system visually and graphically.

Therefore, it would have been obvious to combine Dunn's embedded display with Yoshiba's display memory control system to obtain the invention as specified in claim 4.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Katsura et al. (US 4,947342) discloses a graphic processing system for storage and delivery of characters in the form of pixel unit information and is suitable for high speed processing when developing characters at given positions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Neil R. McLean whose telephone number is 571. 270.1679. The examiner can normally be reached on Monday through Friday 7:30AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, King Poon can be reached on 571.272.7440. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Neil R. McLean
1/06/2007

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